PROPOSED CLAIM AMENDMENTS

As discussed, applicant respectfully requests that Examiner Li consider the attached set of proposed amendments to the claims

1. (PROPOSED) An execution unit for execution of multiple context threads, comprising:

an arithmetic logic unit to process data for executing threads;

control logic to control the operation of the arithmetic logic unit; and

a general purpose register set to store and obtain operands for the arithmetic logic unit, the register set comprising a plurality of two-ported random access memory devices assembled into banks, the register set comprising two effective read ports and one effective write port, wherein the effective write port comprises the write ports of a pair of the two-ported random access memory devices, each bank being capable of performing a read and a write to two different words in the same processor cycle,

wherein the arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port.

15. (PROPOSED) A method for executing multiple context threads, comprising:

processing data for executing threads within an arithmetic logic unit;

operating control logic to control the arithmetic logic unit; and

storing and obtaining operands for the arithmetic logic unit within a general purpose register set comprising a plurality of banks of two-ported random access memory devices, the register set comprising two effective read ports and one effective write port, wherein the effective write port comprises the write ports of a pair of the two-ported random access memory devices, the effective write port including a single write line to write to addresses in different banks of the plurality of banks, and each bank being capable of performing a read and a write to two different words in the same processor cycle.

19. (PROPOSED) A processor unit comprising:

an execution unit for execution of multiple context threads, the execution unit comprising:

an arithmetic logic unit to process data for executing threads;

control logic to control the operation of the arithmetic logic unit;

a general purpose register set to store and obtain operands for the arithmetic logic unit, the register set comprising a plurality of two-ported random access memory devices, the register set comprising two effective read ports and one effective write port, wherein the effective write port comprises the write ports of a pair of the two-ported random access memory devices; and

a data link between the arithmetic logic unit and the one effective write port of the general purpose register set, wherein the data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port.